

Principal Digital ASIC Engineer

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Company: Ixana

Location: Bengaluru

Category: other-general

Note This position requires 3 + years of industrial experience in RTL Design. If your skillset is

a) Physical Design: Do Not Apply

b) RTL Verification: Do Not Apply

c) Feel free to email hello@ixana.ai with resumes in these cases. But, do not apply via

LinkedIn unless you have 3+ year experience in RTL Design and have tapeout

experience. Company ixana.ai is a Purdue University spinoff, developing brain-inspired

wearable computing. We have assembled a team of leading experts in the field of IC/system

design with an appetite for taking on the next big thing. Come join us in the journey of

transforming the future with high-speed human-computer interfaces that amplify your

potential with all-day real-time AI. Come join us in the journey of transforming the

future. Why should you be excited? You have heard of Bluetooth, you have heard of Wi-Fi,

Ixana has developed a fundamentally new wireless technology, Wi-R which is 100x lower

energy than Bluetooth/Wi-Fi. Check out ixana.ai for videos on how Wi-R streams high speed

data through your skin. See a video of our disruption here:

<https://vimeo.com/ixana/pairing-contact-transfer> Team and Role Overview

We are seeking a senior RTL Design Engineer to join our IC Design team. As a senior RTL Design Engineer, you

will be responsible for and lead digital signal processing hardware designs, specifically data path

as well as control intensive digital designs. You will work with or as the System architect, as

well as other ASIC designers to micro-architect and implement low-power

communication system designs integrated into our SoC. Required Qualifications: Bachelor's

degree in Science, Engineering, or related field.

5+ years ASIC design, verification, or related work experience.

Strong skills in RTL logic design (VHDL or Verilog) and verification

Should have extensively used RTL Linting tools and extensive usage of simulation tools.

Experience with ASIC ECO flow, RTL sanity tools specific to Design Rule Checking and Clock

Domain Crossing checks

Familiarity with MBIST and DFT flow

Gate level Simulation debug and usage of power extraction tools a plus Preferred

qualifications:Tcl/Perl/Python shell-scripting skills

Experience with digital signal processing is a bonus

Knowledge of different wireless communication circuits is a plus

Outstanding communication and documentation skills

Experience with multi-power domain design using UPF

Power aware simulations using VCS-NLP or similar tools

Experience using STA, PNR tools

Experience with Hardmacro integration in RTL The position is based in our Bengaluru

(Marathahalli) office. PS: Ixana's booth number at CES 2023 was 61305.

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