

## Sr. Principal Design Engineer - FE

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Company: L&T Semiconductor Technologies

Location: Bengaluru

Category: architecture-and-engineering

### RoleSr. Principal Design Engineer - FE

Str[REDACTED]opment for Mobility, Industrial, Energy & Telecom

Reporting ToChief Development Officer / Global Head of Engineering

LocationBengaluru

### COMPANY DESCRIPTION

[REDACTED]

L&T Semiconductor Technologies (LTSCT), a fully owned subsidiary of L&T, is the first major Indian Semiconductor product company a fabless company for designing & delivering Smart Devices for Global Customers. A company that provides Semiconductor Devices and Technology partnerships by helping customers realise energy efficient, high performance systems to benefit from data, electrification and software defined technology trends.

Harnessing the engineering mastery of L&T, LTSCT is forging a path to a worldclass semiconductor ecosystem rooted in India. We aim to rewrite the rules of cutting-edge technology through relentless innovation to foster a vibrant culture of ingenuity, fuelling progress on every chip.

We have a presence in four prominent geographies i.e. US, Europe, Japan and India, with offices in Austin, Munich, London, Tokyo, Bangalore and Chennai.

### JOB DESCRIPTION

[REDACTED]

LTSC's Chief Development Organization and Global Engineering team is a central engineering organization responsible for developing and delivering Systems-on-a-Chip (SoCs) for LTSC's Automotive, Industrial, Energy and Telecom infra business lines. The team is challenged to produce industry leading solutions covering very cost sensitive, low power devices to highly integrated, high performance, multidomain devices compliant with the latest automotive and industrial safety and security standards.

### **AREAS OF RESPONSIBILITY:**

Lead a SoC FE team to own SoC integration of a complex ARM architecture based SoC upto RTM

Manage a high impact FE team and take accountability for their timely deliverables

Interact and engage early on with SoC system architect and ensure performance analysis, functional safety requirements, system level use cases and pin mixing is fully comprehended

Drive complete SoC integration, LEC, LINT checks and CDC/RDC analysis to ensure high quality deliverables.

Responsible for ensuring power intent of the SoC is understood and implemented correctly through LowPower checks like CLP.

Ownership of power estimation through the cycle and responsible for meeting/beating active and leakage power targets for the device in different modes

Collaborate with systems, IP and DV teams to align on feature updates, bug fixes, IP deliverables and ensure timely SoC integration releases that cater to Product Requirements

### **Qualifications :**

Educational requirement Bachelor or Masters in EE/ECE/CS or related specializations with 15+years of experience in IP/SoC/subsystem design/integration

## Skills :

Experience with integration of SoC's with ARM processors, complex bus architectures

Well experienced with analysis and understanding of system level use case scenarios, safety requirements etc

Experience with SoC power analysis and power optimization through innovative schemes

Strong experience with advanced low power techniques and tools such as UPF/CPF, CLP

Good understanding of constraints development for Physical Design implementation / Static Timing Analysis

Experience with industry standard FrontEnd tools like JasperGold, SpyGlass, LEC etc

Well experienced with EDA tools such as VCS/Quarta/Incisive simulators, Debug tools and Formal verification tools

Good understanding of SoC Debug architectures, Design for Debug, Design for Test will be highly desirable.

Strong written and verbal communication skill with the ability to explain and present complex ideas

Passionate about mentoring and developing people in their careers

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