

## STA/Synthesis Engineer

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Company: Wipro

Location: Bengaluru

Category: other-general

Title: STA/Synthesis Engineer

Location: Bengaluru or Hyderabad

Description:

1. Performing Timing closure of partitions at SoC level
2. Providing placement feedback with respect to timing
3. Reduction of clock ID, by analyzing necessary tap points
4. Providing clock pulls and pushes to attain better QoR before going to ECOs to reduce leakage/utilization impact
5. Fixing setup, Hold, TDRCs, Noise through ECOs

Should have hands on tolls knowledge in:

HDL's: Verilog, VHDL

EDA Tools: PTSI, Tempus, Tweaker, ICC2, Innovus, DCG/DCT

Scripting Languages: Exposure to Perl, Shell, Tcl, Makefile

Operating Systems: Windows, Linux

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